R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found on page 8, lines 15-17 of the Specification as filed. No new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-4, 6, 7 and 10 under 35 U.S.C. §103 as being unpatentable over Scheck in view of Wrape et al. has been is respectfully traversed and should be withdrawn.

Scheck teaches a system and method for reducing clock skew sensitivity of a shift register (Title). Wrape et. al teach a testable integrated circuit with reduced power dissipation (Title).

In contrast, claim 1 of the present invention concerns an apparatus comprising one or more groups of boundary scan cells, one or more group buffers coupled to each of the groups of boundary scan cells, one or more repeater buffers coupled in series with the group buffers, a controller coupled to the groups of boundary scan cells through the group buffers and the repeater buffers. The apparatus is configured to buffer the groups of boundary scan cells

to reflect an order of I/Os around the apparatus and (ii) the groups of boundary scan cells are routed within an I/O portion of said apparatus to avoid routing through an interior portion of the apparatus to keep the interior portion free for functional routing. The one or more flip flops are each configured to provide a scan enable output. The scan enable signal is configured to control a scan connection between each of the flip flops.

Scheck does not teach or suggest the claimed boundary scan cells are routed within an I/O portion of the apparatus to avoid routing through an interior portion of the apparatus to keep the interior portion free for functional routing. Scheck appears completely silent regarding routing boundary scan cells within the I/O portion. Wrape also appears silent regarding routing boundary scan cells within the I/O portion. Since neither Scheck nor Wrape teach such routing, it follows that neither Scheck nor Wrape teach the claimed limitation "to keep the interior portion free for functional routing". Clearly, Wrape fails to cure the deficiencies of Scheck. Therefore, the references, alone or in combination, fail to teach the presently claimed invention and the rejection should be withdrawn.

Claim 6 is believed to be independently patentable over Scheck. In particular, claim 6 provides that each boundary scan cell of the groups of boundary scan cells are implemented within an I/O cell. Scheck is silent regarding the embedding of the boundary

scan cells in the I/O cells. It is unclear how the remarks on page 5 of the Office Action relate to claim 6. At best, the reference in Scheck to a dout in FIG. 4A refers to a boundary scan cell output. However, such an output does not teach or suggest a group of boundary scan cells implemented within an I/O cell, as presently claimed. Therefore, claim 6 is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-4 and 6-10 depend, directly or indirectly, from claim 1, which is now believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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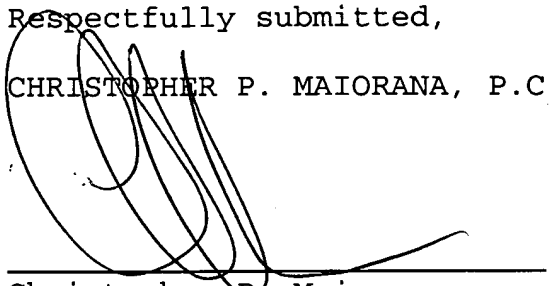

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